

Open**TRANSPUTER**

Reinventing a parallel machine from the past

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About me...

- ▶ Andrés Amaya García
- ▶ Graduated from the University of Bristol in 2015
- ▶ MEng Computer Science

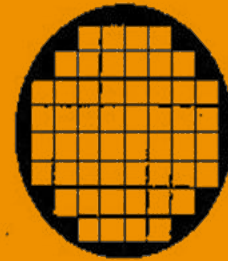


“

Once upon a time,
nine (rainy) months
ago...

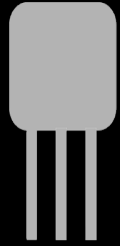
The Transputer

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inmos

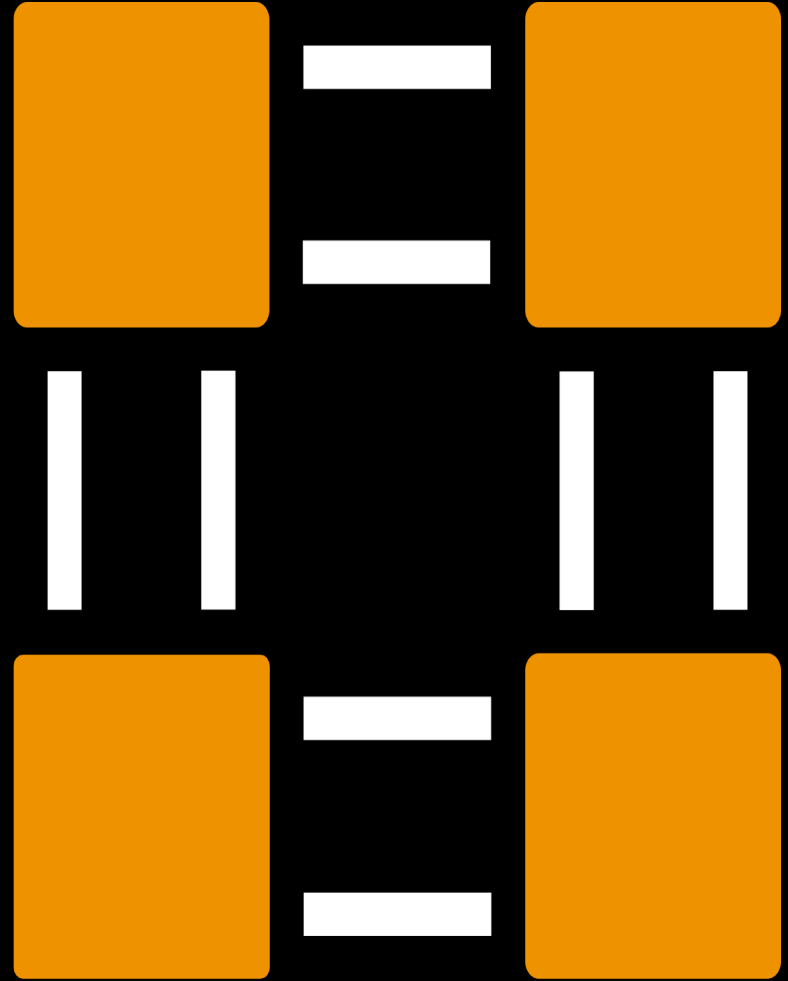




Transistor



Transputer



System

Transputer applications

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Amstrad TV set-top box contains ST20

Transputer applications

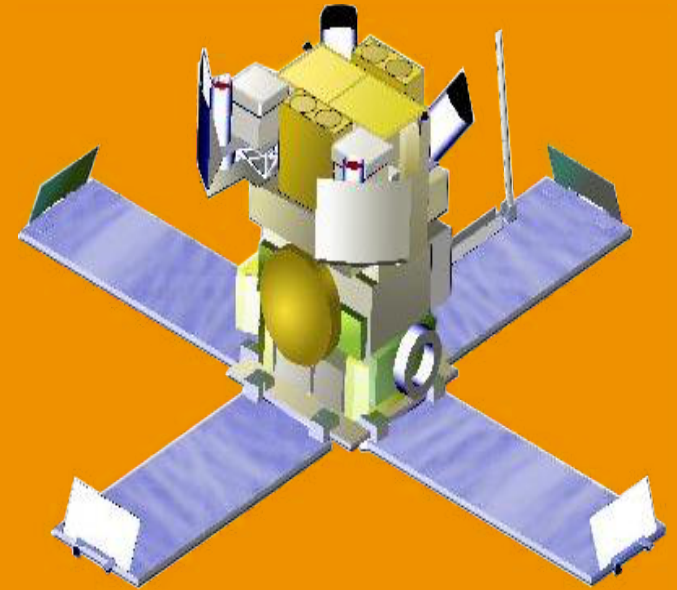
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Transputer applications

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Amstrad TV set-top box contains ST20



HETE-2 contains T805 Transputers

Project objectives

Project objectives

- ▶ Open-source.

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- ▶ Supports Transputer instruction set.

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- ▶ Supports Transputer instruction set.
- ▶ Different micro-architecture.



The Internet of Things (IoT) is all about connectivity!

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- ▶ Open-source.
- ▶ Supports Transputer instruction set.
- ▶ Different micro-architecture.
- ▶ New external communication mechanism and I/O interface.

How does the Transputer work?

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Occam

- ▶ Occam is a high-level programming language developed at Inmos hand-in-hand with the Transputer.
- ▶ Explicit concurrency and interprocess communication.

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“

The Devil is in
the detail

Microcomputer Division Confidential

Author: Roger Shepherd

```
WHILE active
  VAL INT interruptable IS GotoSNPBit /\ (IOBit /\ (MoveBit /\
                                     (TimeInsBit /\ TimeDelBit))) :
  SEQ
  -- completed indicates if current instruction has terminated
  completed := (StatusReg /\ interruptable) = 0
  validProcess := Wptr <> NotProcess.p

  PRI ALT
  (StatusReg /\ GotoSNPBit) <> 0 & SKIP
  StartNextProcess ()

  (Priority = 0) AND (NOT (TNextReg[0] AFTER ClockReg[0])) AND
  completed & SKIP
  HandleTimerRequest (0)

  ALT hc = 0 FOR LinkChans
  (Priority = 0) AND completed & FromChan[hc][0] ? token
  HandleChannelRequest (token, hc)

  (Priority = 1) AND
  (NOT (TNextReg[0] AFTER ClockReg[0])) & SKIP
  HandleTimerRequest (0)

  ALT hc = 0 FOR LinkChans
  (Priority = 1) & FromChan[hc][0] ? token
  HandleChannelRequest (token, hc)

  (Priority = 1) AND (NOT (TNextReg[1] AFTER ClockReg[1])) AND
  completed & SKIP
```

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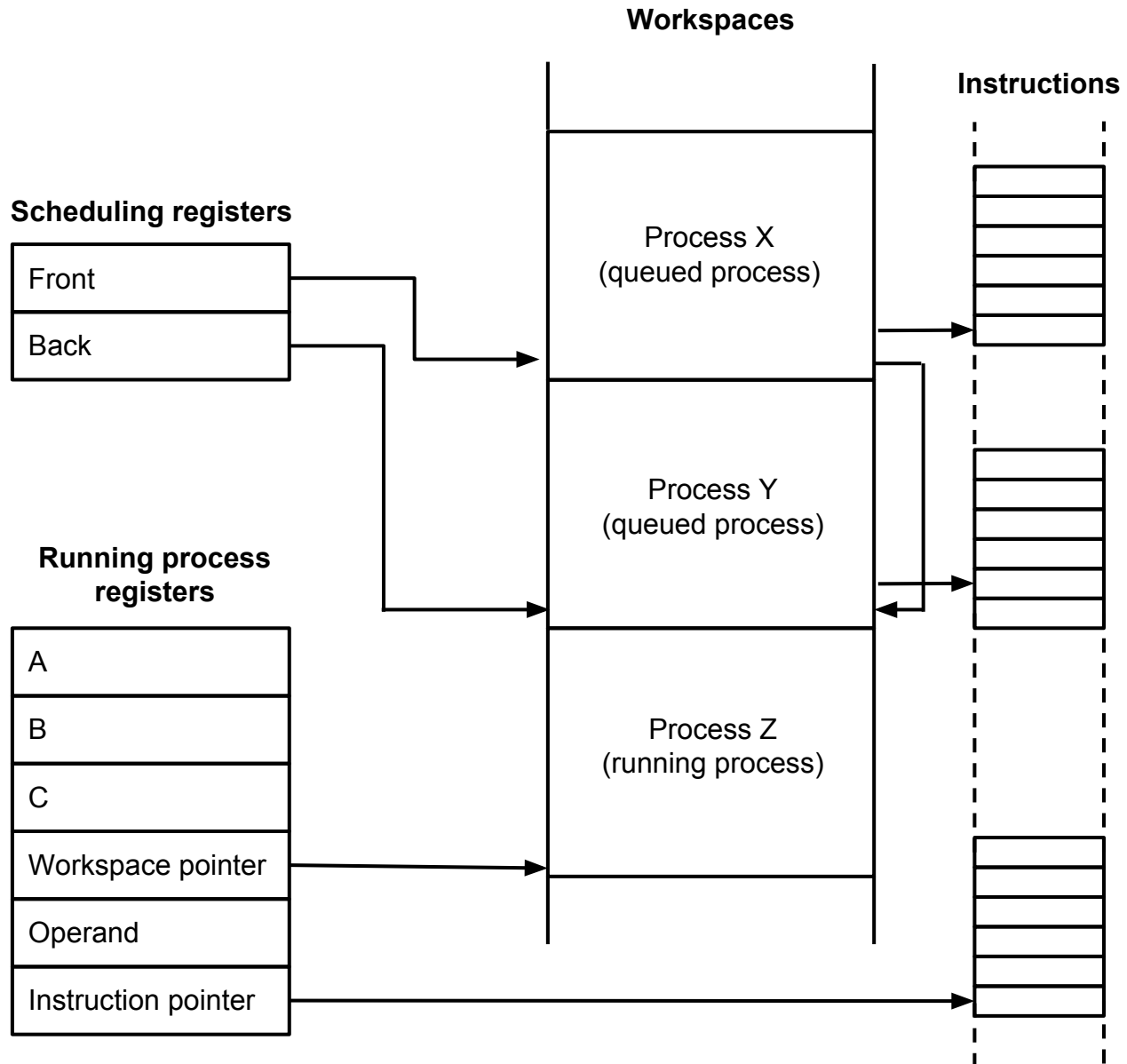
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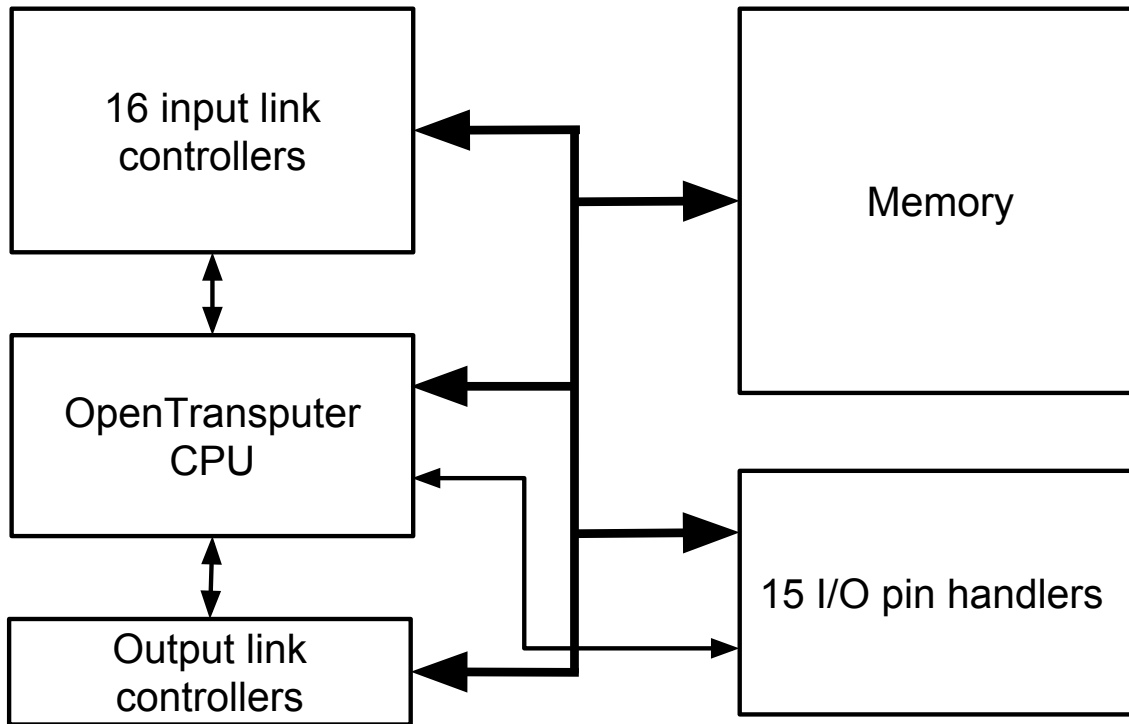
Interprocess communication

- ▶ Special Transputer instructions implement Occam primitives efficiently.
- ▶ Communication performed either through channel in memory or physical links.

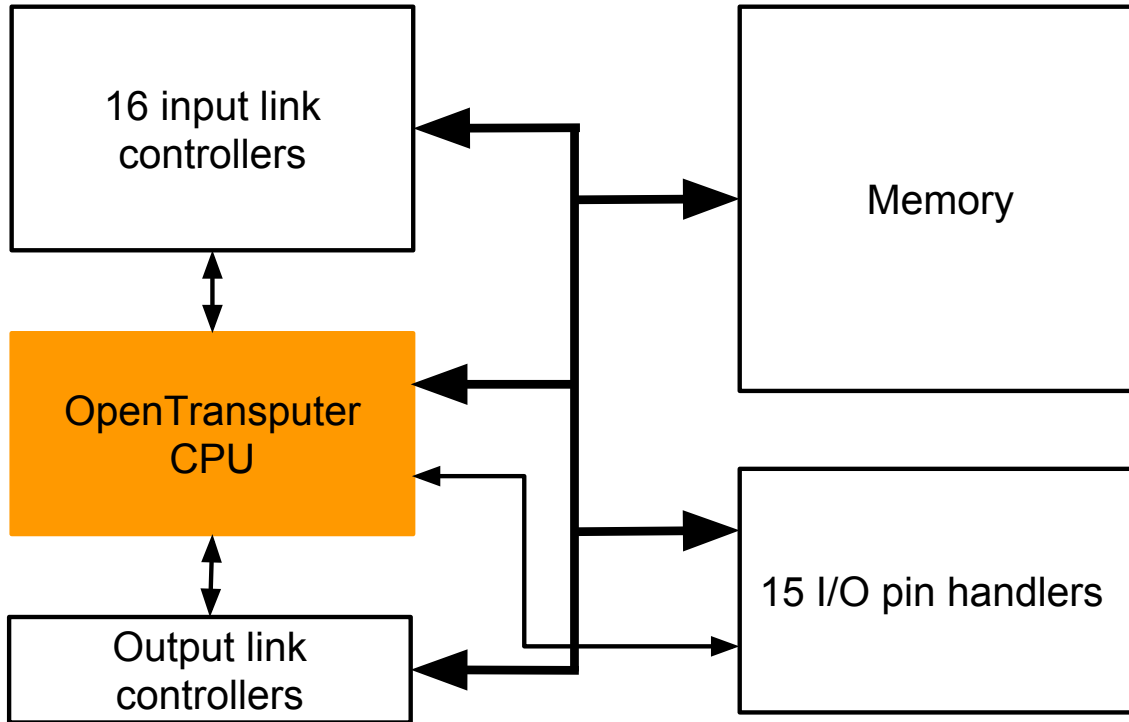
But I want to
hear about the
OpenTransputer!

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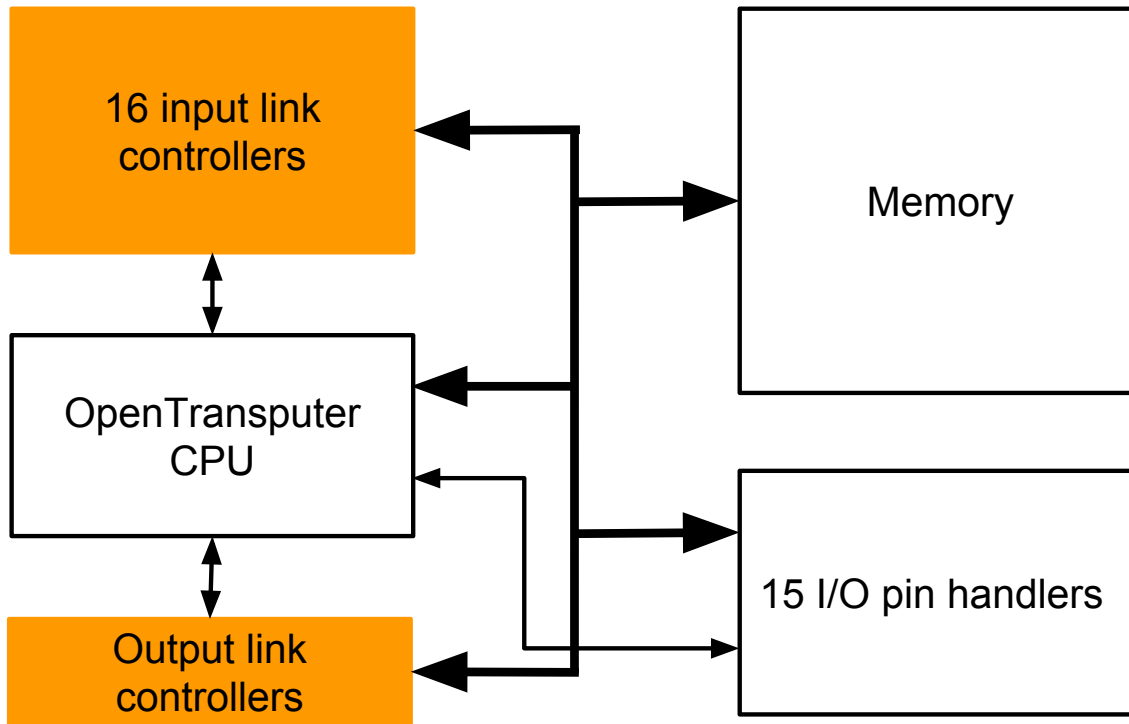
Processor components



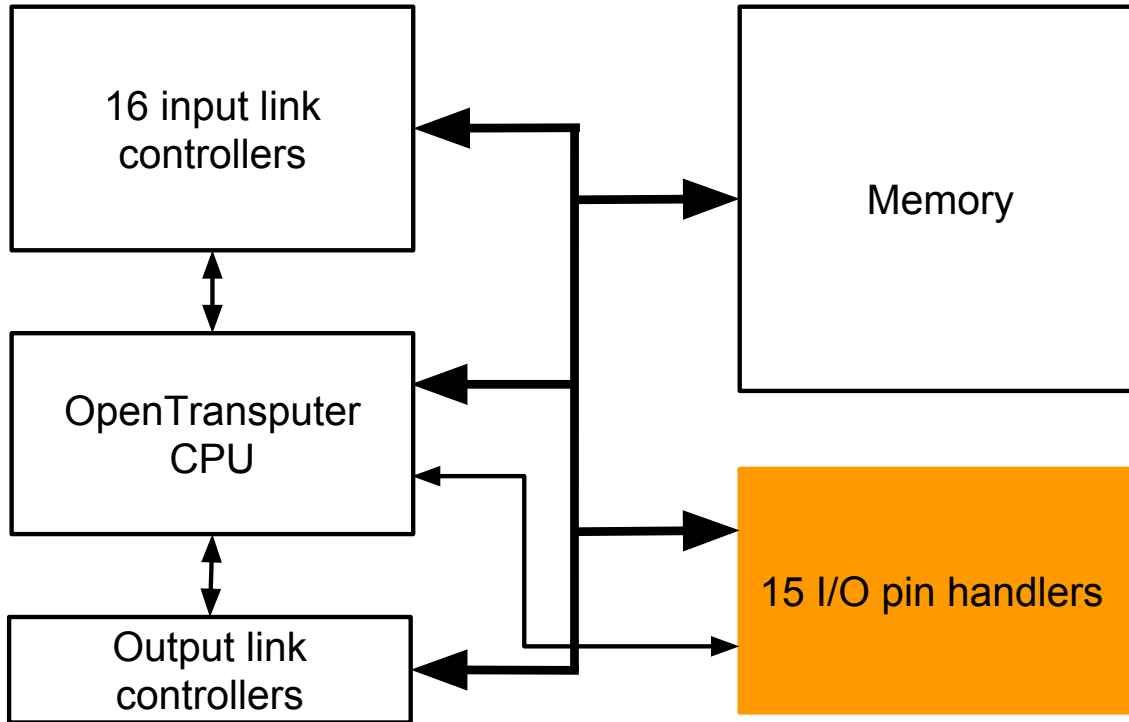
Processor components



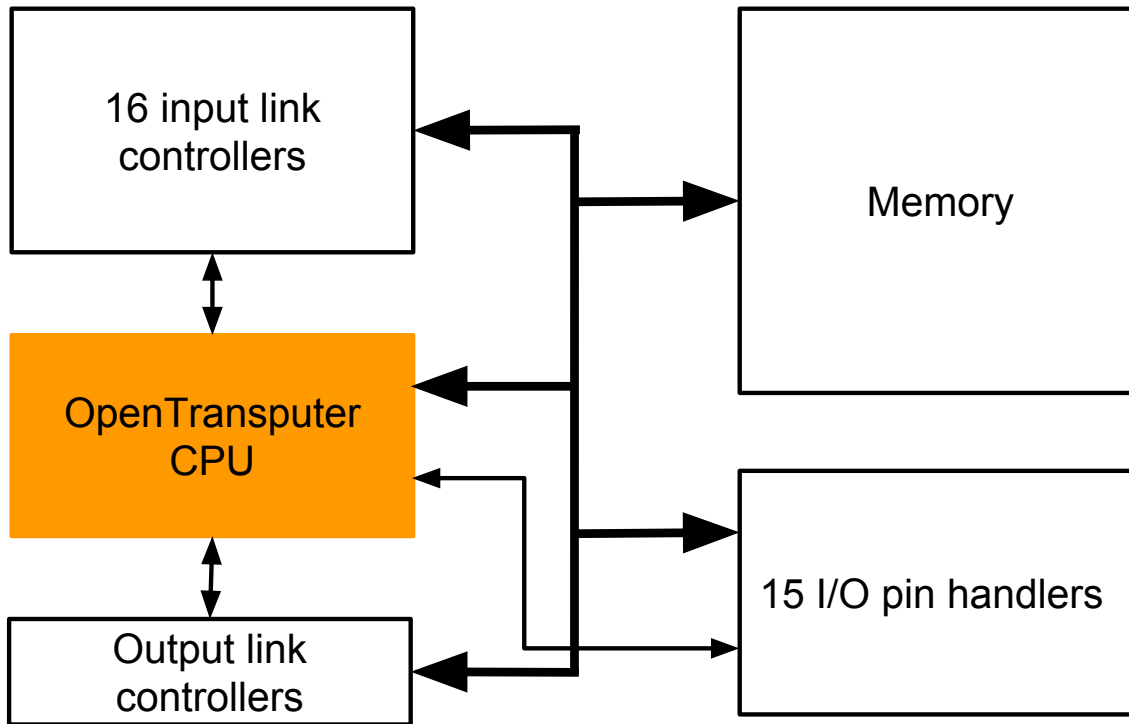
Processor components



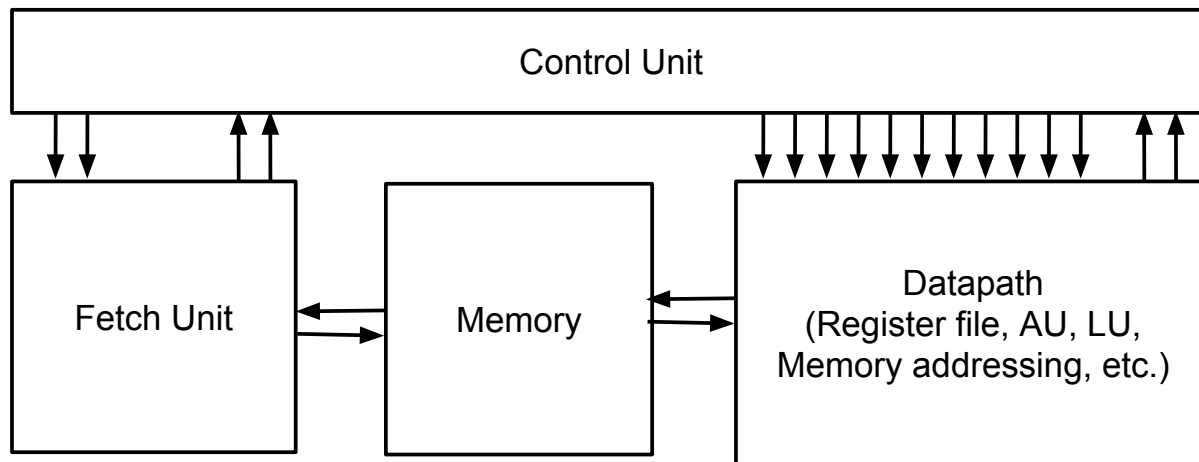
Processor components



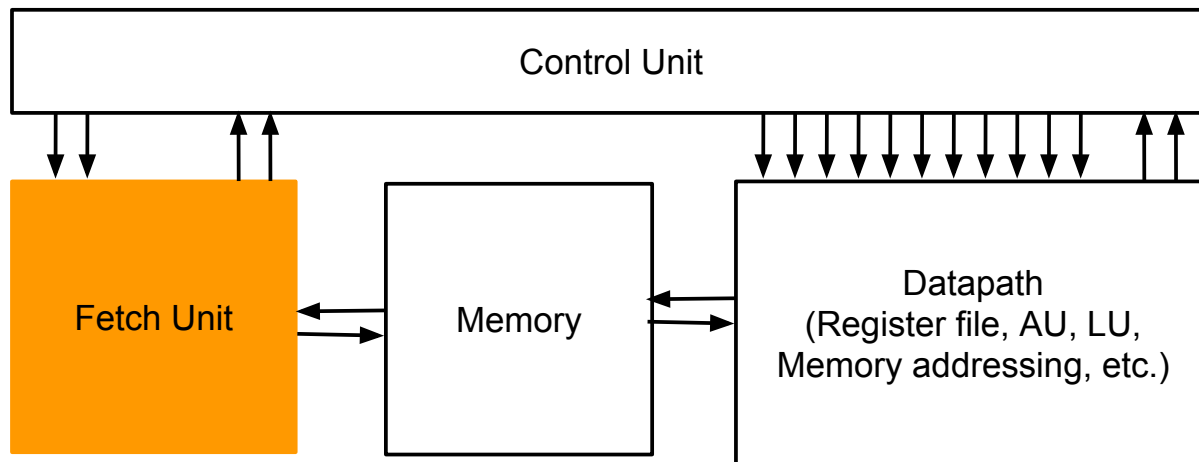
Processor components



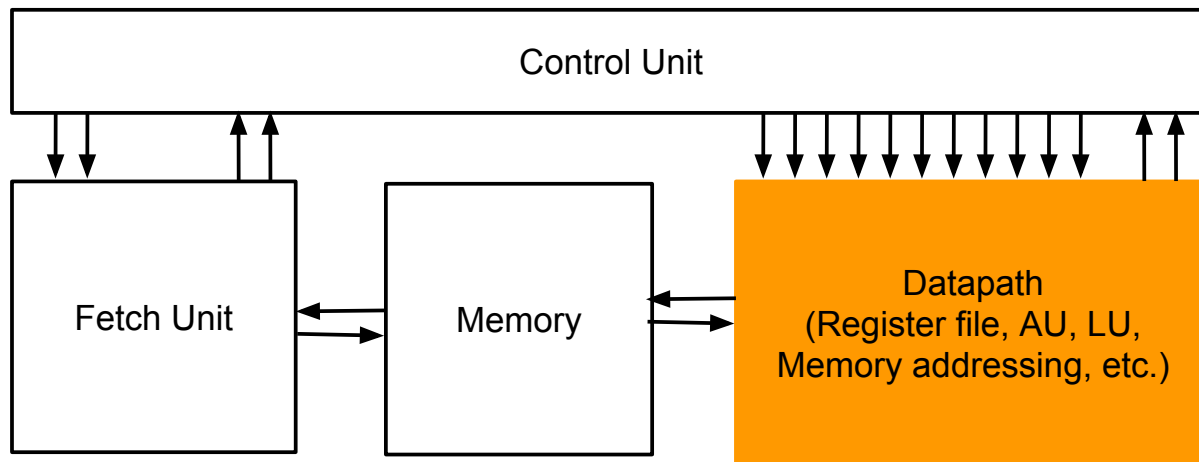
CPU



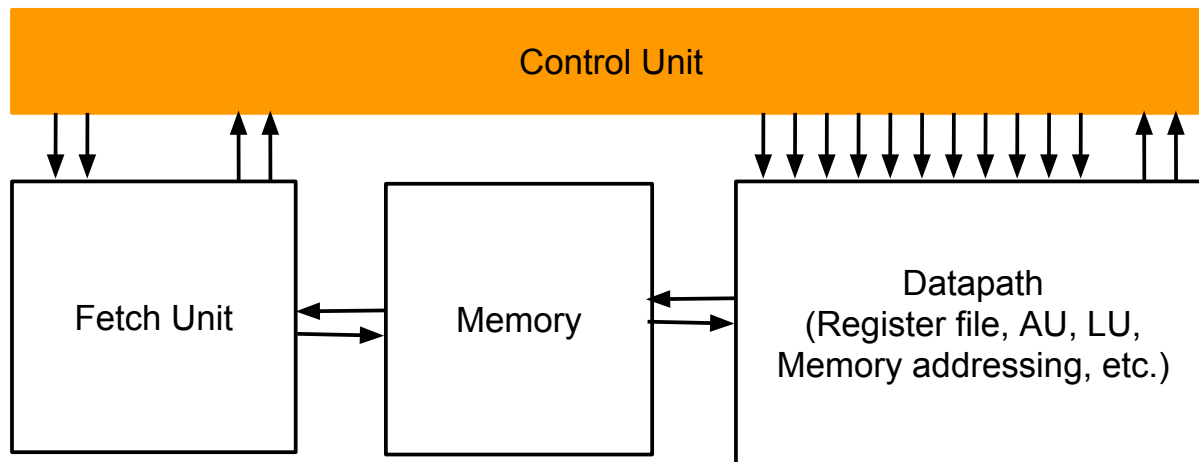
CPU



CPU



CPU



Control unit

Inmos Transputer

- ▶ Microcoded control unit.
- ▶ Control signals stored in Read-Only Memory (ROM).
- ▶ Area savings and potentially less complex.

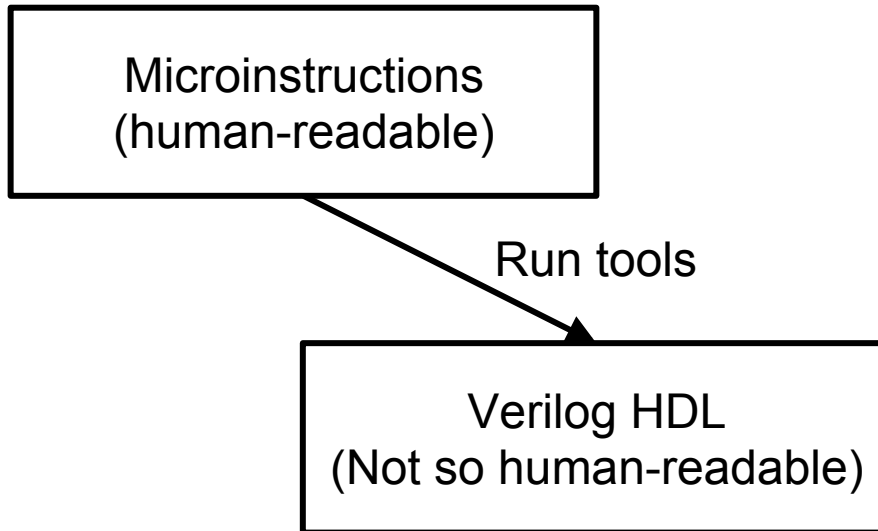
OpenTransputer

- ▶ Designed with a microcode strategy.
- ▶ Control signals generated by hardwired logic.
- ▶ Potentially faster than ROM.

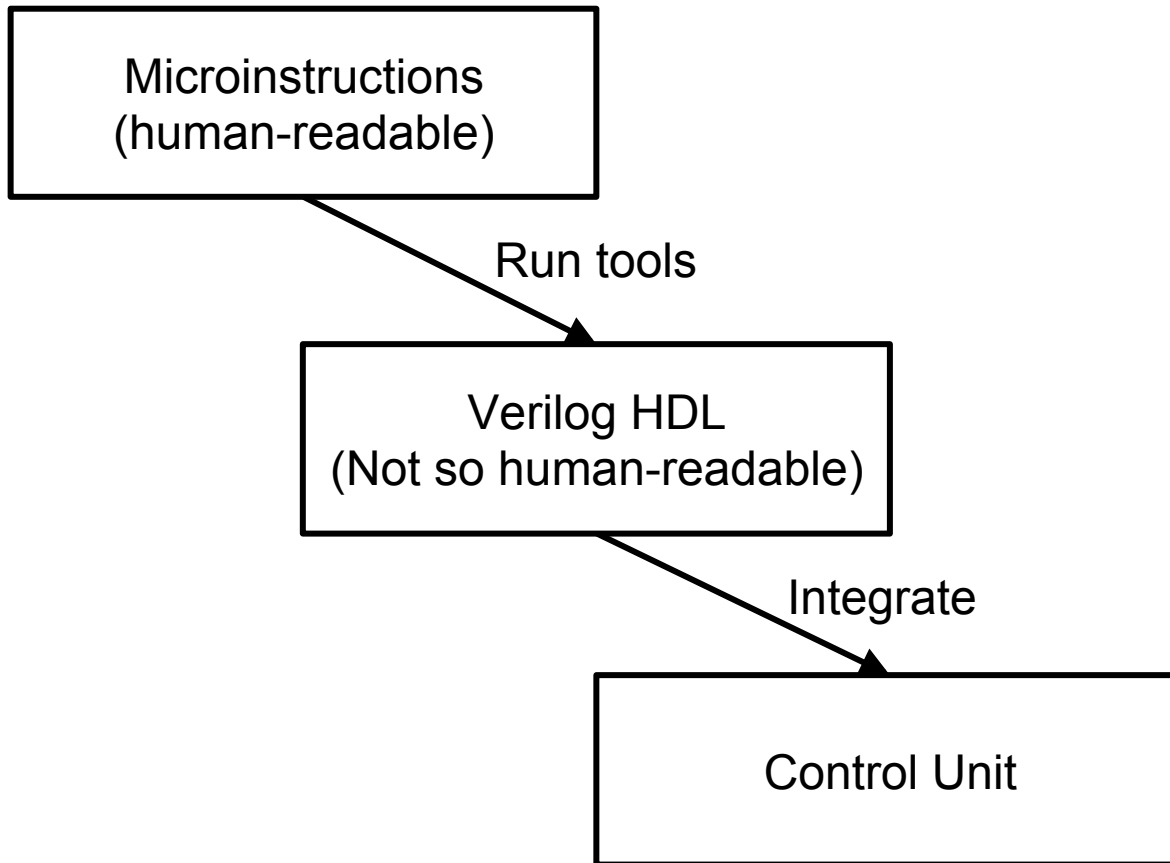
Control unit

Microinstructions
(human-readable)

Control unit



Control unit

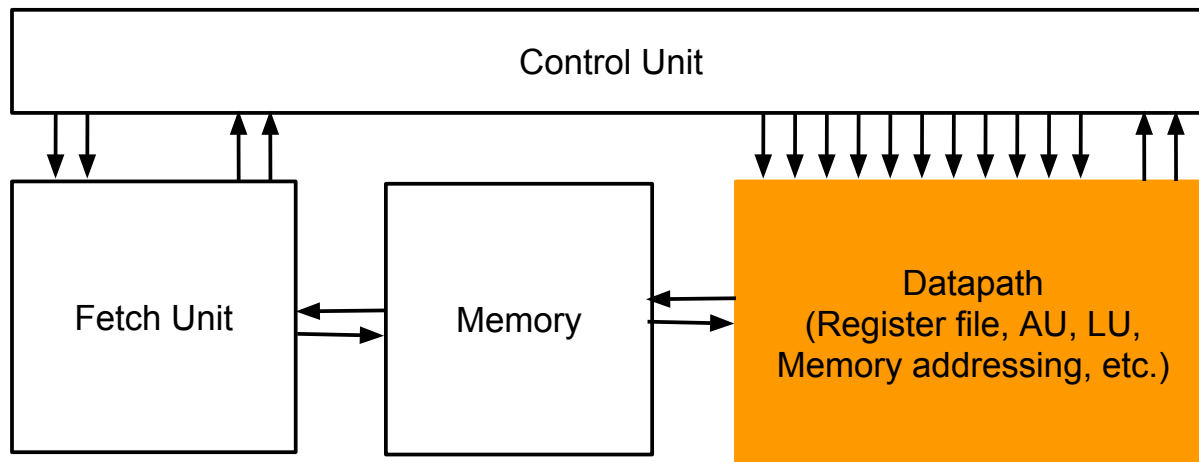


OpenTransputer microinstructions

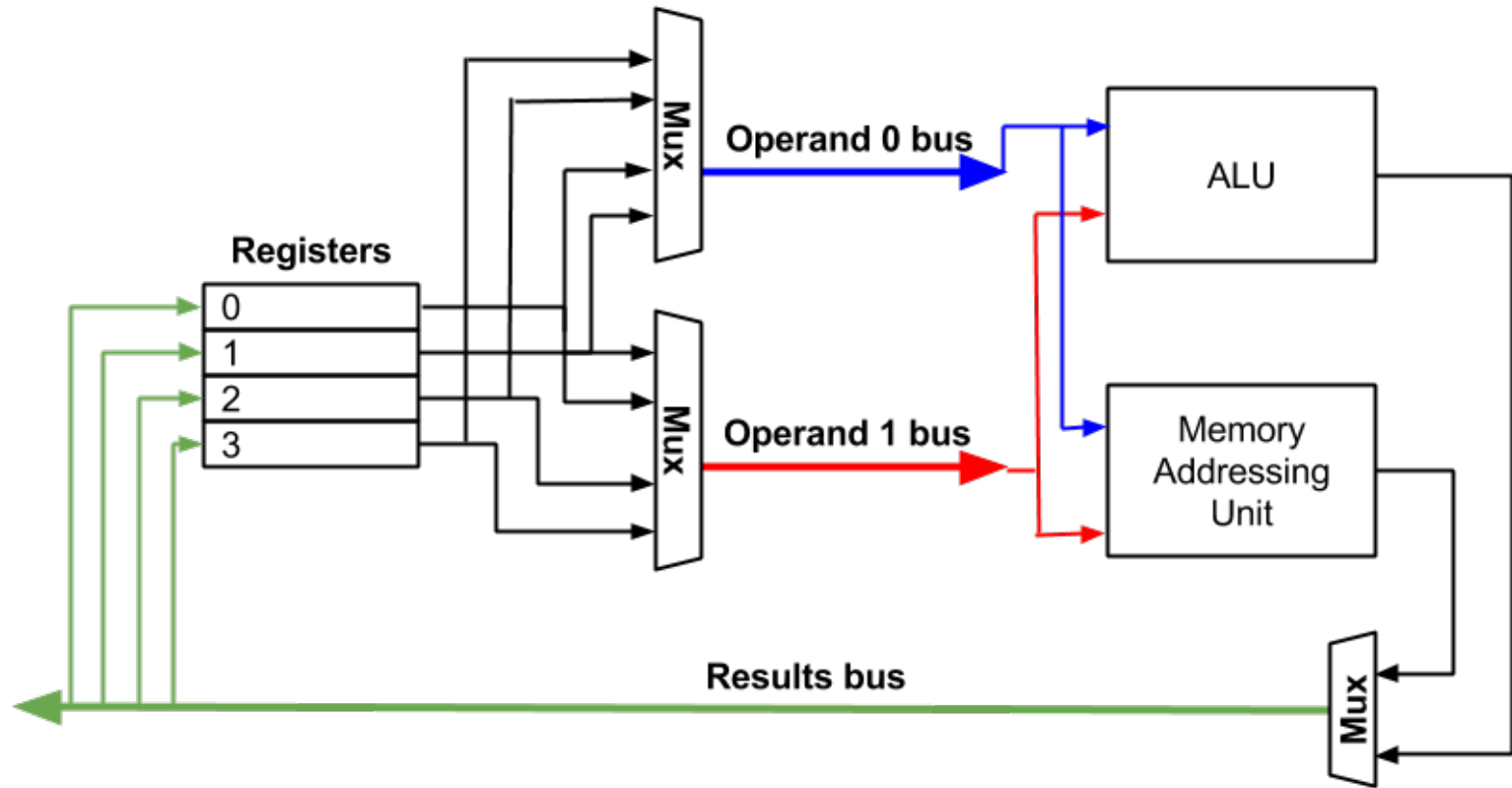
CJ0 ROMp0(0)
CmpconstfromA
Conda11(CJ1,CJ2);

CJ1 AfromB
BfromC
OfromClear
Gotoplus1;

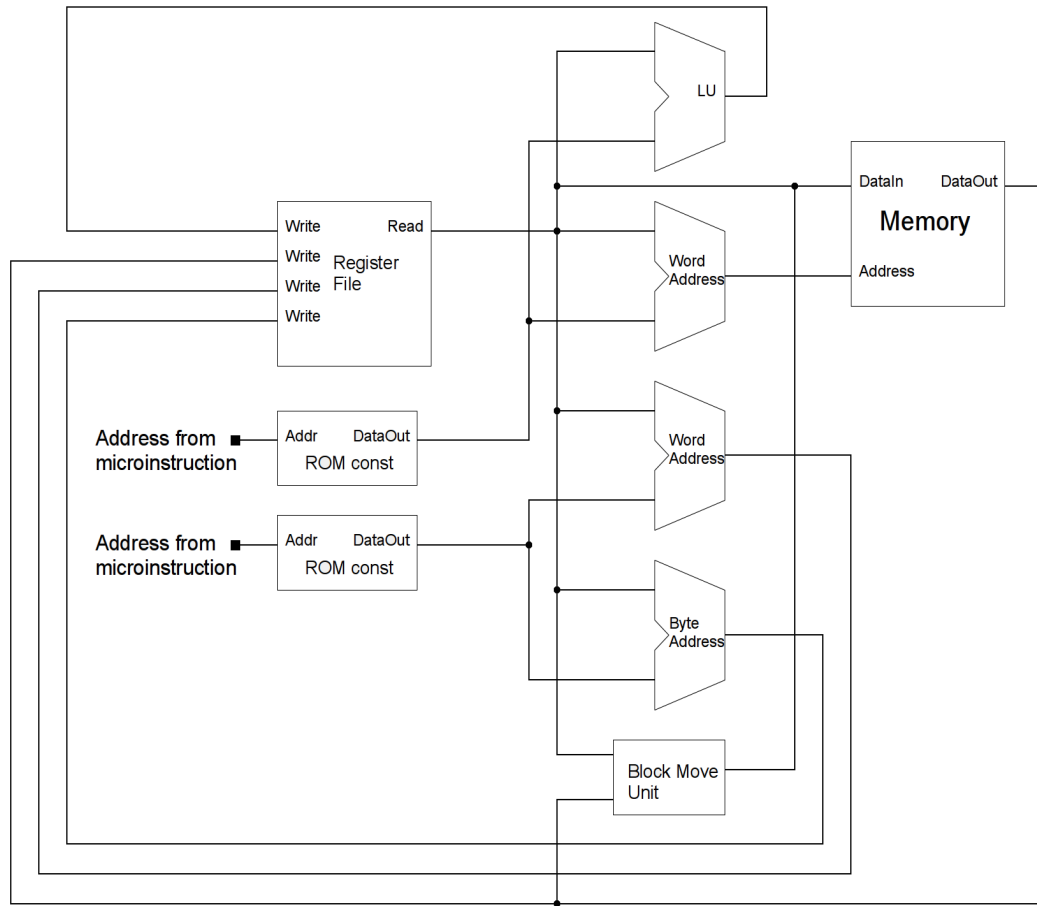
CPU



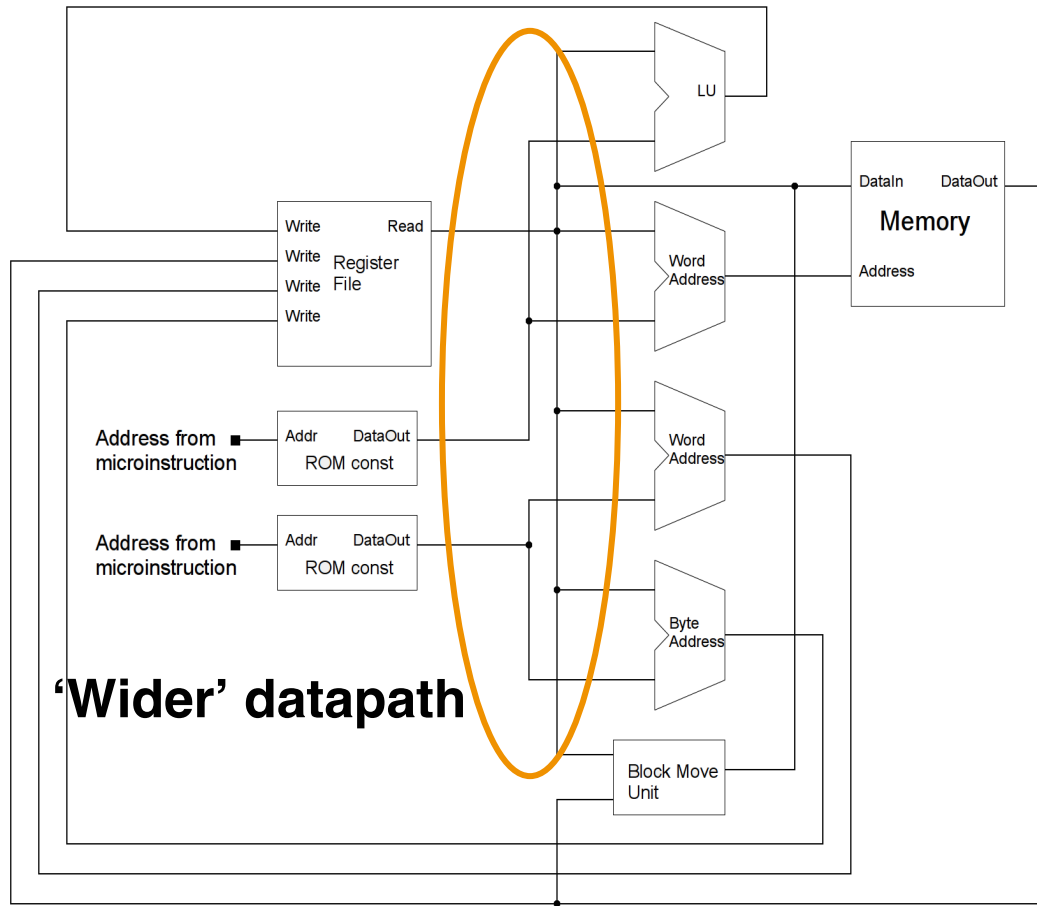
Inmos Transputer datapath



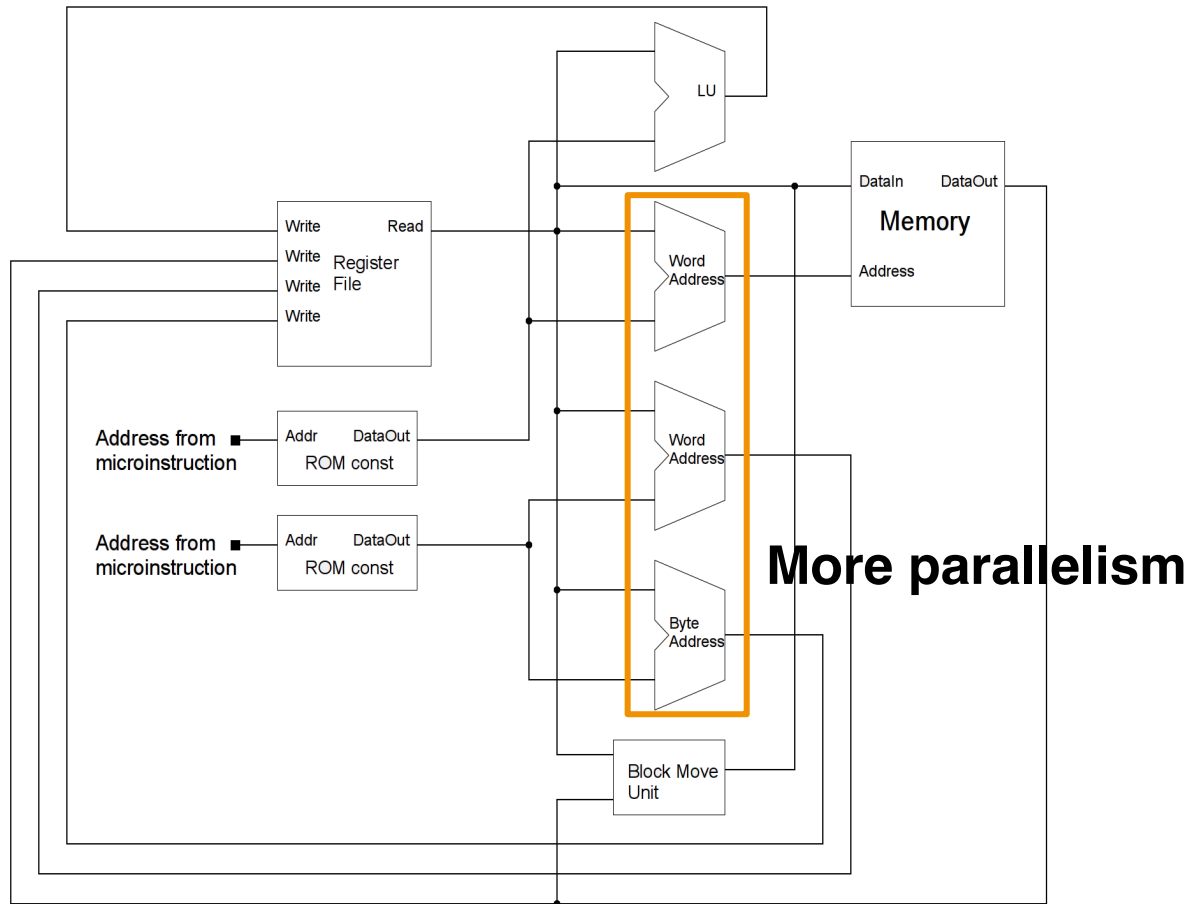
OpenTransputer datapath



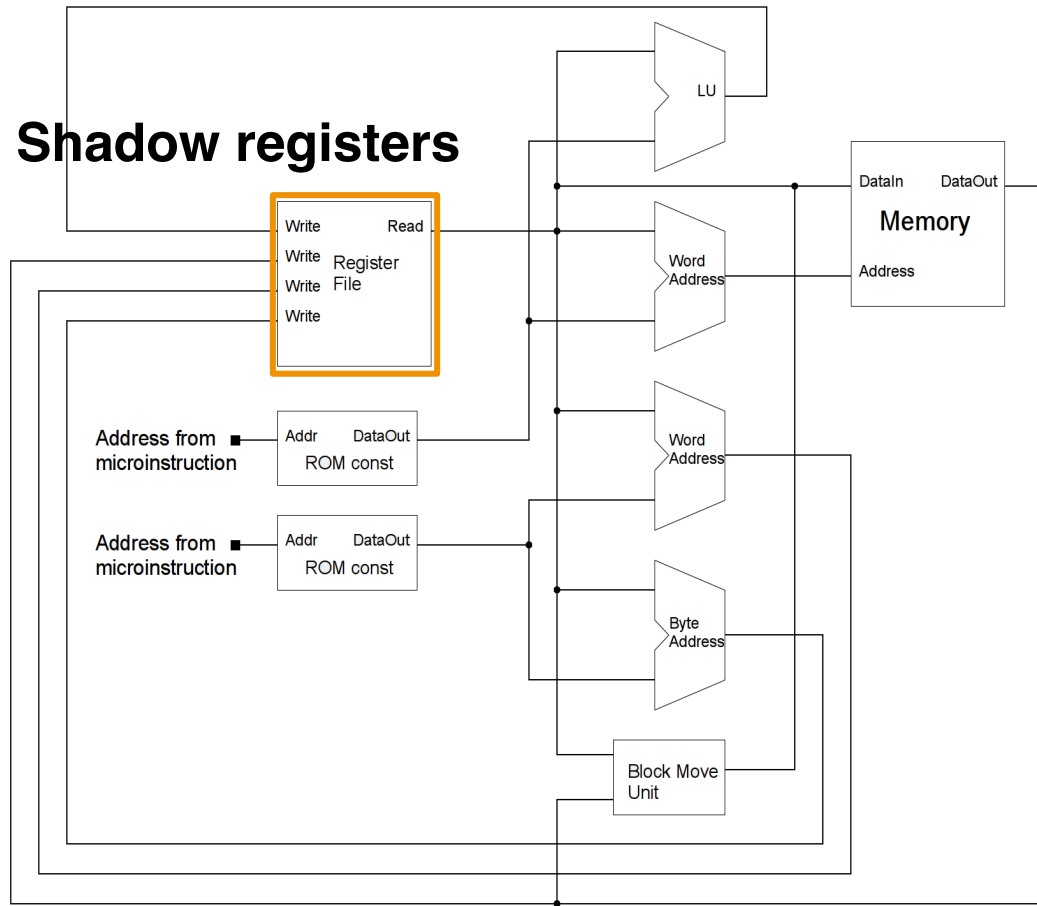
OpenTransputer datapath



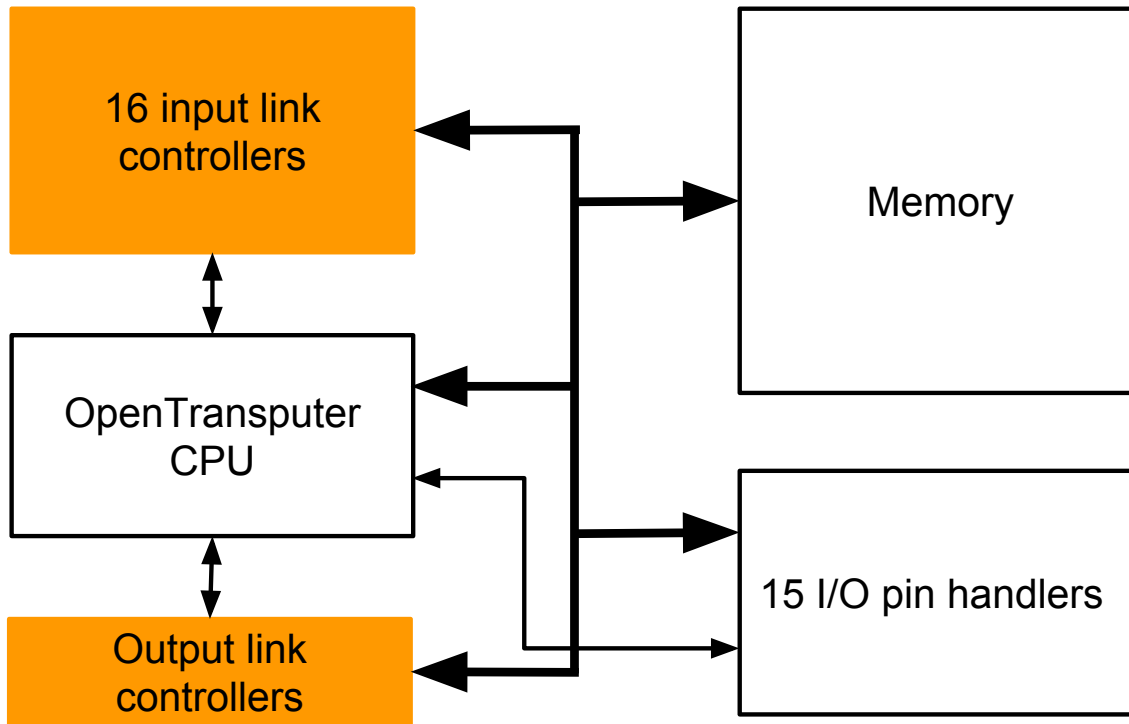
OpenTransputer datapath



OpenTransputer datapath

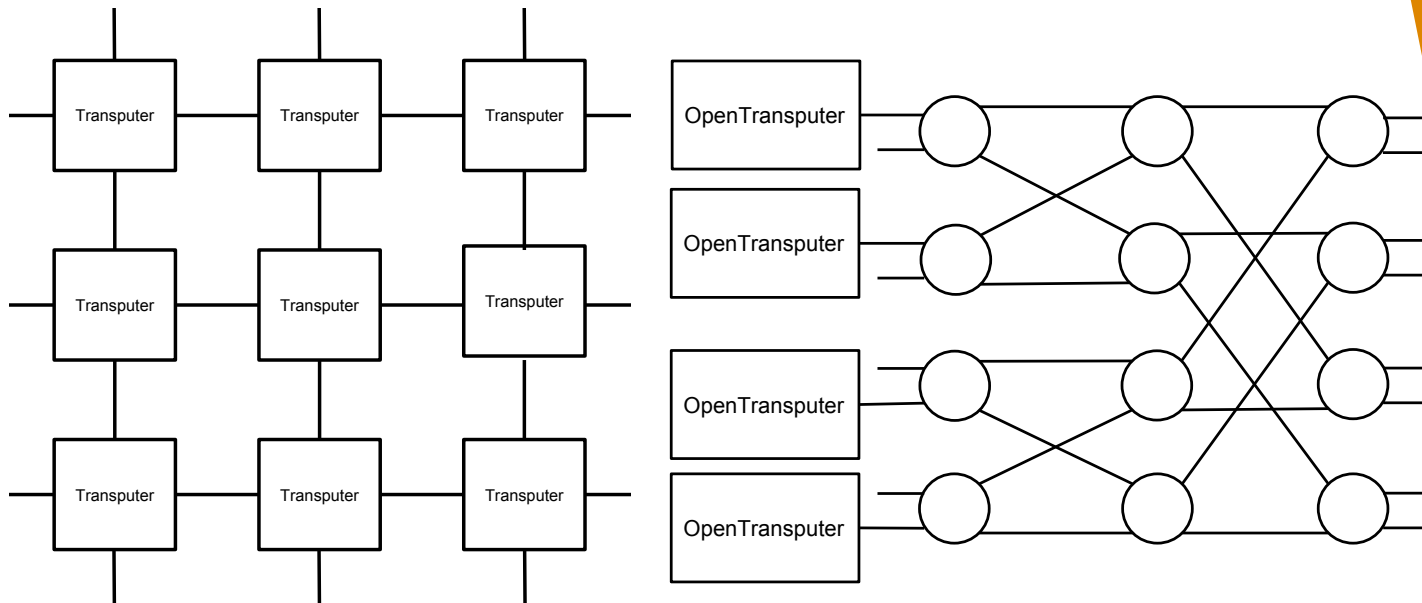


Processor components



External communication

Inmos Transputer OpenTransputer

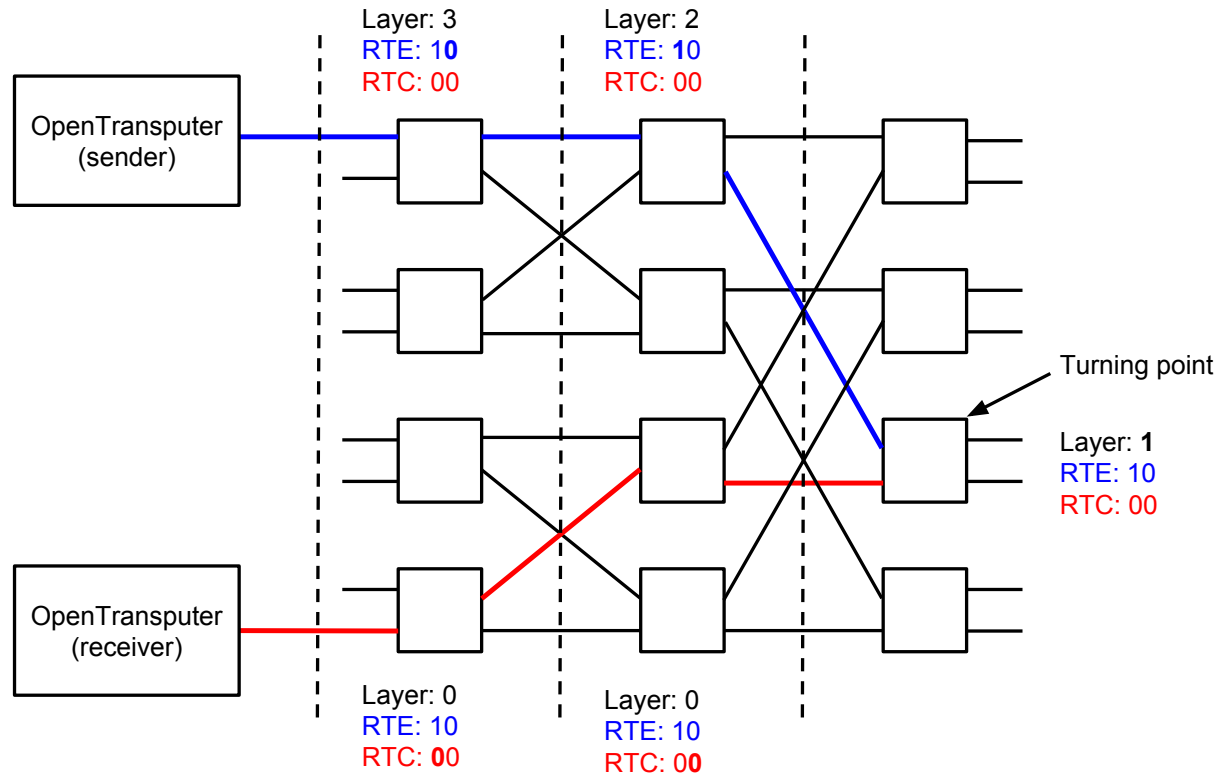
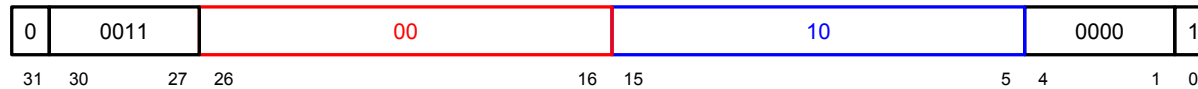


Autonomous link controllers

- ▶ There are 16 input ports and a single output port.
- ▶ Extended the original Transputer controllers to support *virtual channels* allowing an arbitrary number of processes to be queued to perform output operations.

Message routing

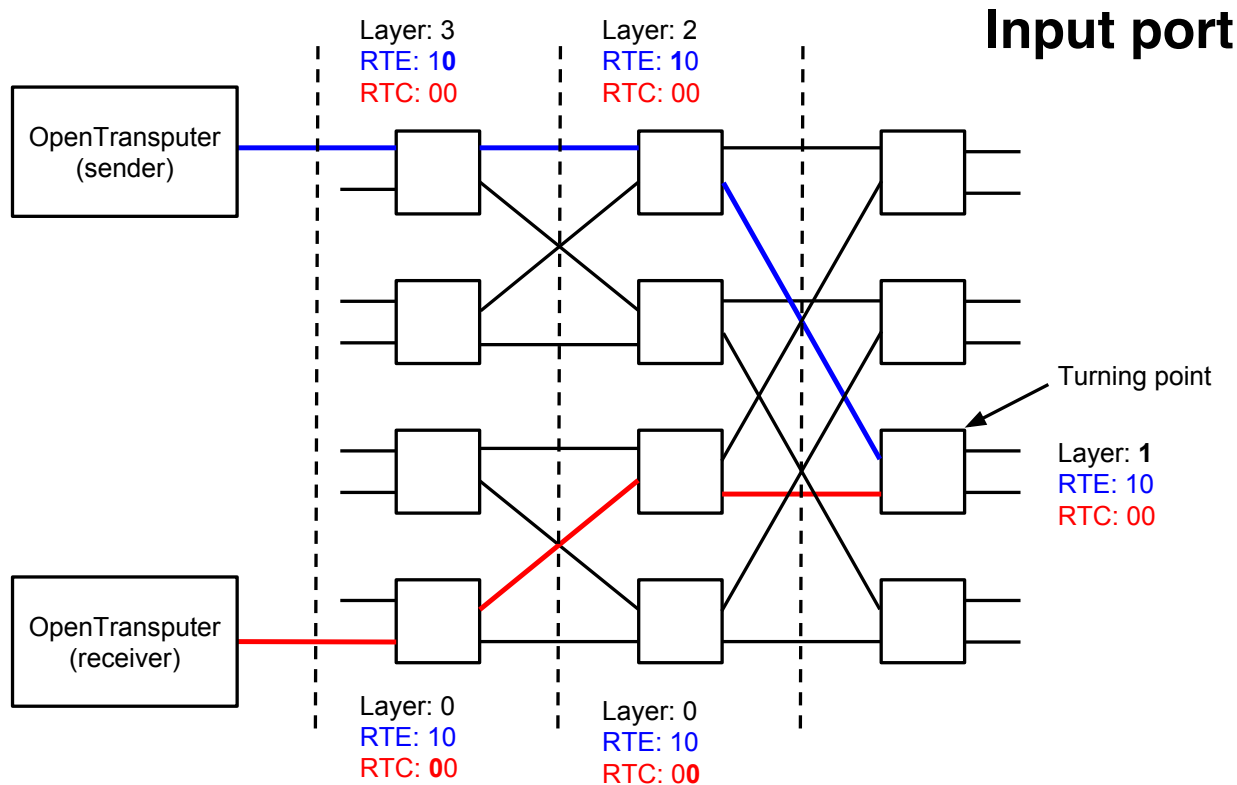
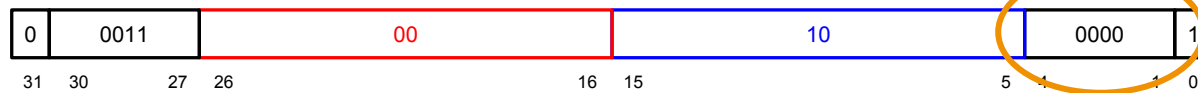
Initial address



- Route towards edge (RTE)
- Route towards core (RTC)

Message routing

Initial address

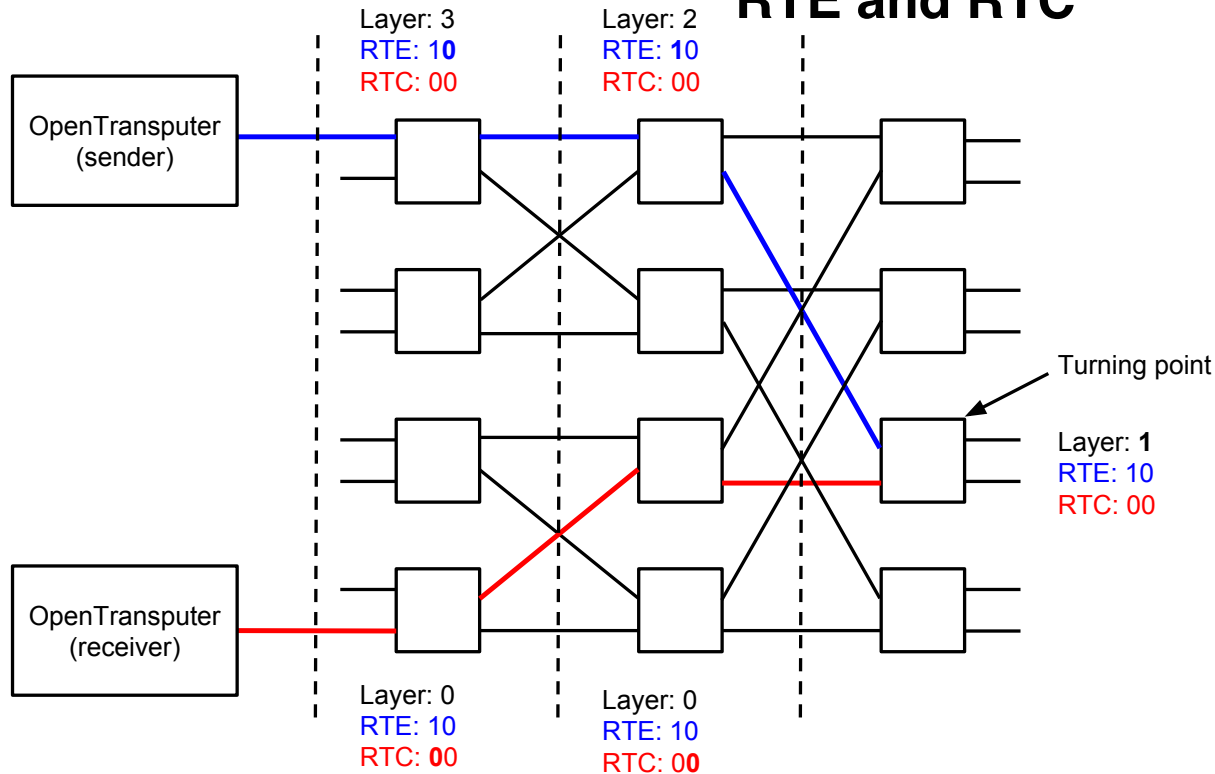


Message routing

Initial address



RTE and RTC

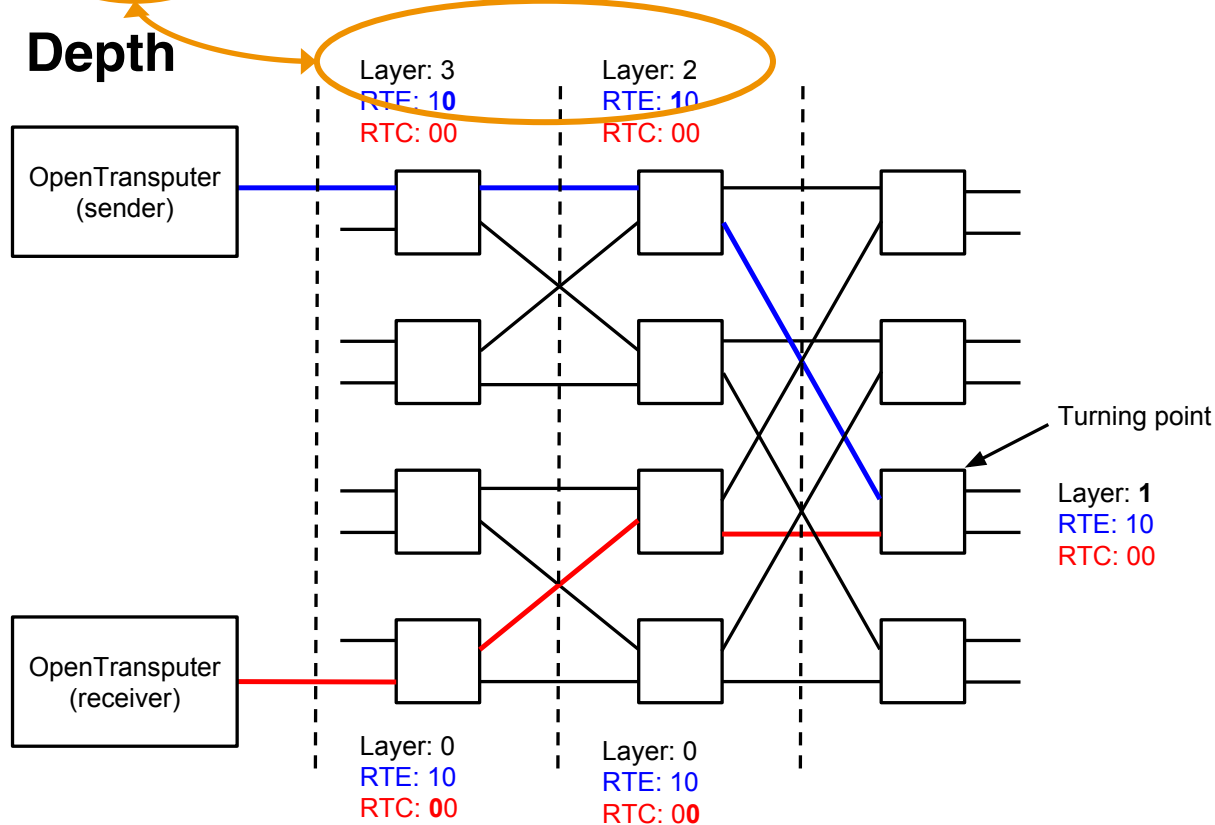


Message routing

Initial address

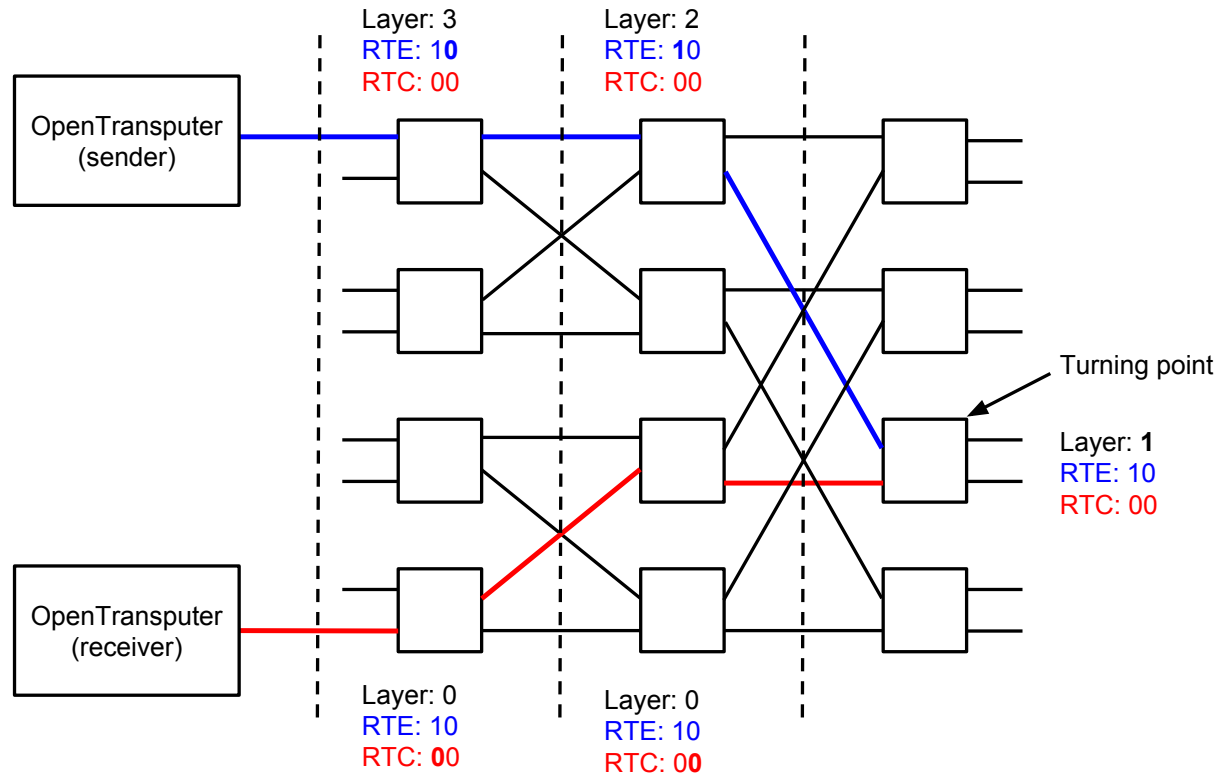
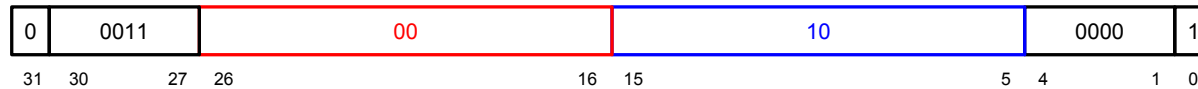


Depth

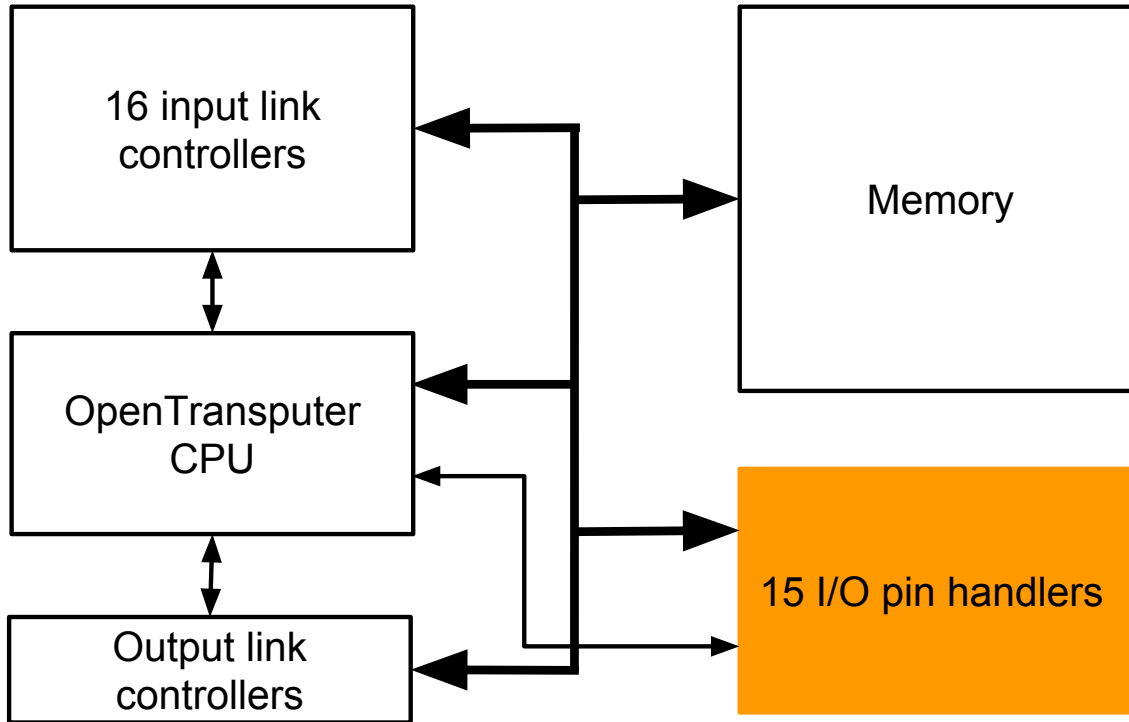


Message routing

Initial address



Processor components



OpenTransputer I/O interface

- ▶ I/O pins expose the same interface as communication links.
- ▶ Introduced an instruction (`confio`) that can be used to configure the I/O pins.

So... what about
performance?

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Synthesis

Synthesised design for both the ZedBoard XC7Z020-CLG484 FPGA and a 180nm manufacturing process.



Comparing synthesis results


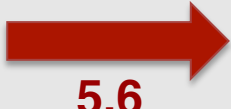
	Inmos Transputer	OpenTransputer
Area	64 mm ²	3.69 mm ²
Manufacturing technology	1000 nm	180 nm

Comparing synthesis results

	Inmos Transputer	OpenTransputer
Area	64 mm ²	3.69 mm ²
Manufacturing technology	1000 nm	180 nm

A red arrow points from 1000 nm to 180 nm with the number 5.6 below it, indicating a 5.6x reduction in technology node size.

Comparing synthesis results

	Inmos Transputer	OpenTransputer
Area	64 mm ²	3.69 mm ²
		
Manufacturing technology	1000 nm	180 nm
		

Comparing cycle counts

Instruction	Inmos Transputer	OpenTransputer
ldl	2	1
startp	12	3-5
endp	13	3
move	$8 + 2w^*$	$6 + 5w^*$

** w is the number of words to copy.*

Conclusion

- ✓ OpenTransputer based on the Transputer architecture.
- ✓ Different micro-architecture to take advantage of modern manufacturing technologies
- ✓ New external communication mechanism.
- ✓ New I/O interface.

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Thank you!

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