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T42 – Transputer Design in FPGA (Year Two Design Status Report)

Fringe Presentation

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Abstract. This fringe session will present the design progress of our IMS-T425 compatible Transputer design in FPGA. The 32-bit CPU + Memory interface (2x8kB) are in stable working condition. 117 instructions (from 123+7) are almost implemented in 460 lines of uCode: for example, `TASM` loops including interruptible `MOVE`(s) can be simulated some 100 clock cycles. Timer(s) are running. The System control unit allows error mode, `MOV`-bit and events. Some still open questions around scheduler micro-code and link interaction will be discussed.

Keywords. T42, transputer, FPGA, scheduler, micro-code, links

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