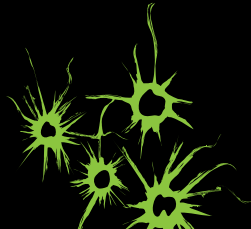


Asynchronous Readers and Writers

A Half-Synchronous Operator





Overview

Introduction of the \Downarrow together with the \downarrow and \Downarrow

\downarrow and \Downarrow versus \downarrow and \Downarrow

\downarrow and \Downarrow using \Downarrow

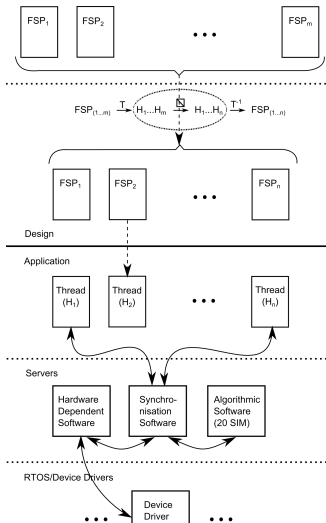
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Semantics of \Downarrow , \downarrow and \Downarrow

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Introduction, system overview





Introduction

- Purpose: Asynchronous Writing and Reading.



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- ▶ without the requirement that the reading processes must be in a state where they can read the value x over a channel c .



Introduction

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- ▶ In CSP writing over a channel is restricted to two processes interacting synchronously via an action containing the ! and the ?.
- ▶ Proposal: a *half-synchronous action* which allows a process to write a value x over a channel c ,
- ▶ without the requirement that the reading processes must be in a state where they can read the value x over a channel c .
- ▶ Together with a half-synchronous parallel alphabetised operator.



Introduction

Advantages of the half-synchronous operator \Downarrow with half-synchronous actions containing \downarrow or \uparrow :



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Introduction

Advantages of the half-synchronous operator \Downarrow with half-synchronous actions containing i or \bar{i} :

- ▶ it eases the complexity of the design eliminating arguably complex process specifications:
 - it is not necessary to use a buffer process in the model to achieve asynchronous writing and reading,
 - the writes (i) and reads (\bar{i}) are asynchronous, which makes it possible to have an order of writes and reads that, if synchronous ($!$, $?$), would lead to a deadlock,



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- ▶ by reducing the number of actions involved in this asynchronous writing and reading of the processes, improves the performance of the periodic hard real-time application,



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- ▶ by reducing the number of actions involved in this asynchronous writing and reading of the processes, improves the performance of the periodic hard real-time application,
- ▶ in a distributed computing system, for example a processor-coprocessor combination, the waiting time of the processor-coprocessor can be reduced.

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! and ? versus ! and ?

Listing 1: Deadlock due to synchronous writing and reading

$$A = c!x_1 \rightarrow c!y_1 \rightarrow d?x_2 \rightarrow d?y_2 \rightarrow SKIP$$
$$B = c?x_1 \rightarrow d!x_2 \rightarrow c?y_1 \rightarrow d!y_2 \rightarrow SKIP$$
$$AB = A||B$$

! and ? versus ! and ?

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trace: $c.x_1$

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$$AB = A || B$$

trace: $c.x_1$

Listing 2: No deadlock due to asynchronous writing and reading

$$A = c!x_1 \rightarrow c!y_1 \rightarrow d!x_2 \rightarrow d!y_2 \rightarrow SKIP$$
$$B = c!x_1 \rightarrow d!x_2 \rightarrow c!y_1 \rightarrow d!y_2 \rightarrow SKIP$$
$$AB = A \Downarrow B$$

! and ? versus ! and ?

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$$A = c!x_1 \rightarrow c!y_1 \rightarrow d?x_2 \rightarrow d?y_2 \rightarrow \text{SKIP}$$
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$$AB = A \parallel B$$

trace: $c.x_1$

Listing 2: No deadlock due to asynchronous writing and reading

$$A = c!x_1 \rightarrow c!y_1 \rightarrow d!x_2 \rightarrow d!y_2 \rightarrow \text{SKIP}$$
$$B = c!x_1 \rightarrow d!x_2 \rightarrow c!y_1 \rightarrow d!y_2 \rightarrow \text{SKIP}$$
$$AB = A \Downarrow B$$

many possible traces, for example:

$$c!x_1 \rightarrow c!y_1 \rightarrow c!x_1 \rightarrow d!x_2 \rightarrow c!y_1 \rightarrow d!y_2 \rightarrow d!x_2 \rightarrow d!y_2 \rightarrow \text{SKIP}$$



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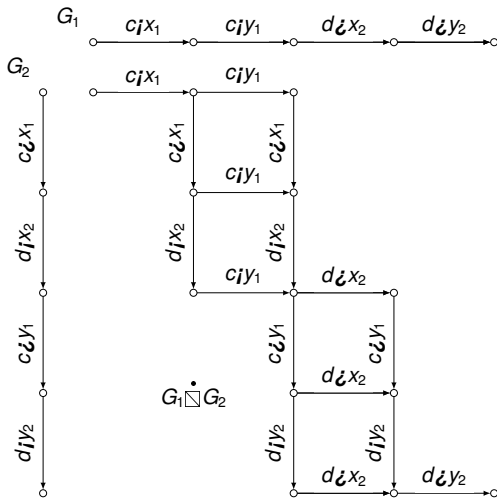
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i and j using \square





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Design Level

Separation of write/read actions in time



Design Level

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Needs a Buffer

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$A = \text{write}.x \rightarrow \text{SKIP}$

$B = \text{read}.x \rightarrow \text{SKIP}$

$\text{Buffer} = \text{write}.x \rightarrow \text{read}.x \rightarrow \text{SKIP}$

$AB = A || B || \text{Buffer}$

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Separation of write/read actions in time
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$AB = A || B || \text{Buffer}$

$A = c_i x \rightarrow \text{SKIP}$

$B = c_o x \rightarrow \text{SKIP}$

$AB = A \Downarrow B$



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Semantics of \Downarrow , \mathfrak{i} and \mathfrak{z}

$$\frac{P \overset{c\mathfrak{i}x:T}{\rightsquigarrow} P', Q_1 \overset{c\mathfrak{z}x:T}{\rightarrow} Q'_1, \dots, Q_n \overset{c\mathfrak{z}x:T}{\rightarrow} Q'_n}{P \Downarrow Q_1 \Downarrow \dots \Downarrow Q_n \overset{c\mathfrak{i}x:T}{\rightsquigarrow} P' \Downarrow Q_1 \Downarrow \dots \Downarrow Q_n \overset{c\mathfrak{z}x:T}{\rightarrow} P' \Downarrow Q'_1 \Downarrow \dots \Downarrow Q'_n},$$
$$c\mathfrak{z}x:T \notin (X, Z)$$

Semantics of \Downarrow , \mathfrak{i} and \mathfrak{c}

$$\frac{P \overset{c\mathfrak{i}x:T}{\rightsquigarrow} P', Q_1 \overset{c\mathfrak{i}x:T}{\rightarrow} Q'_1, \dots, Q_n \overset{c\mathfrak{i}x:T}{\rightarrow} Q'_n}{P \Downarrow Q_1 \Downarrow \dots \Downarrow Q_n \overset{c\mathfrak{i}x:T}{\rightsquigarrow} P' \Downarrow Q_1 \Downarrow \dots \Downarrow Q_n \overset{c\mathfrak{i}x:T}{\rightarrow} P' \Downarrow Q'_1 \Downarrow \dots \Downarrow Q'_n},$$

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$$\frac{Q_i \overset{c\mathfrak{i}x:T}{\rightarrow} Q'_i, Q_j \xrightarrow{y} Q'_j}{Q_i \Downarrow Q_j \xrightarrow{y} Q_i \Downarrow Q'_j}, y \neq c\mathfrak{i}x:T, c\mathfrak{i}x:T \in (Y_i \cdot Y_j),$$

$$y \notin (X, Y_{k=1, \dots, n, j \neq k}, Z)$$

Semantics of \Downarrow , $\dot{\downarrow}$ and $\dot{\downarrow}$

$$\frac{P \overset{c\dot{\downarrow}x:T}{\rightsquigarrow} P', Q_1 \overset{c\dot{\downarrow}x:T}{\rightarrow} Q'_1, \dots, Q_n \overset{c\dot{\downarrow}x:T}{\rightarrow} Q'_n}{P \Downarrow Q_1 \Downarrow \dots \Downarrow Q_n \overset{c\dot{\downarrow}x:T}{\rightsquigarrow} P' \Downarrow Q_1 \Downarrow \dots \Downarrow Q_n \overset{c\dot{\downarrow}x:T}{\rightarrow} P' \Downarrow Q'_1 \Downarrow \dots \Downarrow Q'_n},$$

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$$\frac{P \rightsquigarrow P', Q_i \overset{c\dot{\downarrow}x:T}{\rightarrow} Q'_i}{P \rightsquigarrow P'}, (\alpha(\rightsquigarrow) \cdot (Y_1, \dots, Y_n, Z)) = \emptyset$$

Semantics of \Downarrow , i and \mathfrak{z}

$$\frac{P \overset{c\mathfrak{z}x:T}{\rightsquigarrow} P', Q_1 \overset{c\mathfrak{z}x:T}{\rightarrow} Q'_1, \dots, Q_n \overset{c\mathfrak{z}x:T}{\rightarrow} Q'_n}{P \Downarrow Q_1 \Downarrow \dots \Downarrow Q_n \overset{c\mathfrak{z}x:T}{\rightsquigarrow} P' \Downarrow Q_1 \Downarrow \dots \Downarrow Q_n \overset{c\mathfrak{z}x:T}{\rightarrow} P' \Downarrow Q'_1 \Downarrow \dots \Downarrow Q'_n},$$

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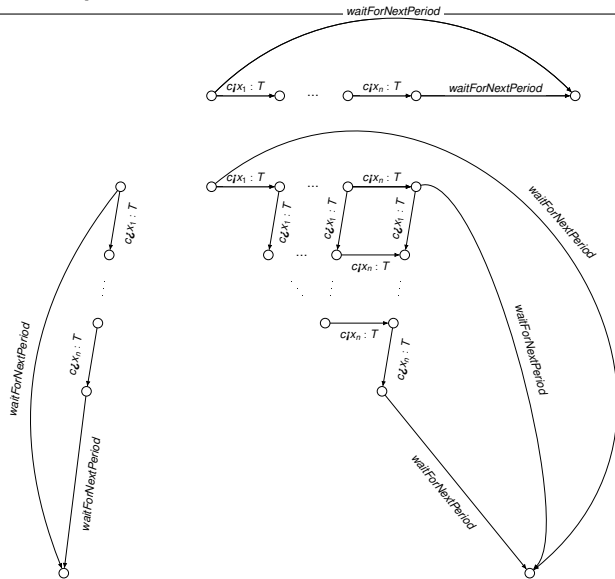
$$\frac{Q_i \overset{c\mathfrak{z}x:T}{\rightarrow} Q'_i, Q_j \overset{y}{\rightarrow} Q'_j}{Q_i \Downarrow Q_j \overset{y}{\rightarrow} Q_i \Downarrow Q'_j}, y \neq c\mathfrak{z}x:T, c\mathfrak{z}x:T \in (Y_i \cdot Y_j),$$

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$$\frac{Q_i \overset{c\mathfrak{z}x:T}{\rightarrow} Q'_i, Q_j \overset{c\mathfrak{z}x:T}{\rightarrow} Q'_j}{SKIP}, i \neq j$$

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Case study

Application = $c_1 ! x_1 : T \rightarrow c_2 ? y_1 : T \rightarrow$
...
 $c_1 ! x_8 : T \rightarrow c_2 ? y_8 : T \rightarrow$
 $display_f(y_1, \dots, y_8) \rightarrow \text{SKIP}$

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Controller = $c_1 ? x_1 : T \rightarrow writeCoProc.x_1 \rightarrow$
 $readCoProc.y_1 \rightarrow c_2 ! y_1 : T \rightarrow$
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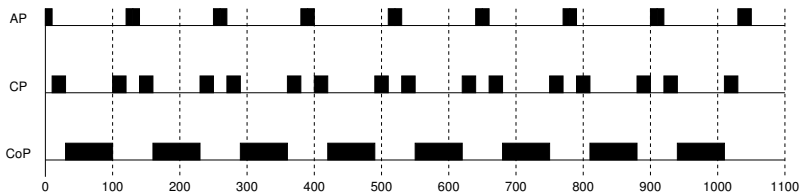
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*System*₁ = $Application_A ||_C Controller$

Example application



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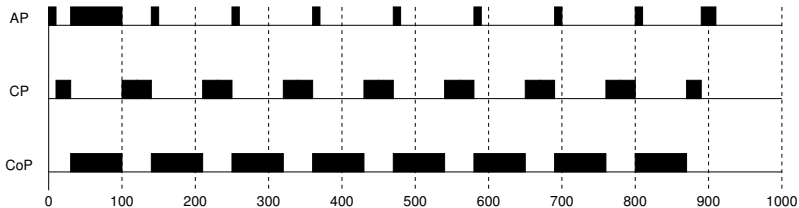
Example application

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Controller = $c_1 \text{ i } x_1 : T \rightarrow writeCoProc.x_1 \rightarrow$
 $readCoProc.y_1 \rightarrow c_2 \text{ i } y_1 : T \rightarrow$
 \dots
 $c_1 \text{ i } x_8 : T \rightarrow writeCoProc.x_8 \rightarrow$
 $readCoProc.y_8 \rightarrow c_2 \text{ i } y_8 : T \rightarrow \text{SKIP}$

$System_2 = Application \downarrow_{A \downarrow C} Controller$

Example application





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- ▶ Index the half-synchronous action such that it is set-wise asynchronous and intra-set-wise synchronous,



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- ▶ Index the half-synchronous action such that it is set-wise asynchronous and intra-set-wise synchronous,
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- ▶ implementation in a tool-chain

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- ▶ elaborate the graph-theoretical characteristics of $\dot{\square}$ (VRSP together with the half-synchronous operator), i.e. it is a commutative monoid of consistent graphs,
- ▶ implementation in a tool-chain and
- ▶ perform a case-study on a periodic hard real-time system.



Thanks!