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Improving the Performance of Periodic Real-time Processes: a Graph Theoretical Approach



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Periodic real-time processes represented by graphs

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- Cartesian product $H_i \square H_j$

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- Performance gain, necessary and sufficient conditions

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- Synchronised product $H_i \square H_j$
- Performance gain, necessary and sufficient conditions
- Future work

Parallel processes represented by graphs

$OBJECT_DISTANCE =$	read_distance_sensors	\rightarrow
	compute_object_distance	\rightarrow
	distance_meas	$\to SKIP$
$ROBOT_SPEED =$	distance_meas	\rightarrow
	compute_robot_speed	\rightarrow
	robot_speed	$\to SKIP$
$MOTOR_SPEED =$	robot_speed	\rightarrow
	compute_motor_speed	\rightarrow
	write_motor_speed_setpoint	$\to SKIP$
$SEQUENCE_CONTROL =$	(OBJECT_DISTANCE	
	ROBOT_SPEED	
	MOTOR_SPEED);	
	SEQUENCE_CONTROL;	

Parallel processes represented by graphs



$$MS = (V(H_1), A(H_1), \{\lambda(a) | a \in A(H_1)\})$$

= ({v₁, v₂, v₃, v₄}, {v₁v₂, v₂v₃, v₃v₄},
{(v₁v₂, rs), (v₂v₃, cms), (v₃v₄, wmss)})

$$RS = (V(H_2), A(H_2), \{\lambda(a) | a \in A(H_2)\})$$

= ({v_5, v_6, v_7, v_8}, {v_5v_6, v_6v_7, v_7v_8}, {(v_5v_6, dm), (v_6v_7, crs), (v_7v_8, rs)})

$$\begin{aligned} OD &= (V(H_3), A(H_3), \{\lambda(a) | a \in A(H_3)\}) \\ &= (\{v_9, v_{10}, v_{11}, v_{12}\}, \{v_9 v_{10}, v_{10} v_{11}, v_{11} v_{12}, \}, \\ \{(v_9 v_{10}, rds), (v_{10} v_{11}, cod), (v_{11} v_{12}, dm)\}) \end{aligned}$$

Cartesian product



MS 🗆 RS 🗆 OD

Weak synchronised product



MS⊟RS⊟OD

Reduced weak synchronised product



Synchronised product intermediate stage



Intermediate stage

Synchronised product



Multi dimensional pathological example



Lemma

Let H_i be an acyclic graph for i = 1, 2, ..., k, where $k \ge 2$. Then $\ell(\Box H_i) = \ell(H_1) + \ell(H_2) + ... + \ell(H_k)$ if and only if every H_i has at least one longest path without synchronising arcs.

Lemma

Let H_i be an acyclic graph for i = 1, 2, ..., k, where $k \ge 2$. Then $\ell(\Box H_i) < \ell(\Box H_i)$ if there exists $H_n, H_m, n \ne m, 1 \le n, m \le k$, such that each longest path in H_n, H_m , contains at least one same labelled synchronising arc.

Theorem

Let H_i be an acyclic graph for i = 1, 2, ..., k, where $k \ge 2$. Then $\ell(\Box H_i) < \ell(\Box H_i)$ if there exists $H_n, H_m, n \ne m, 1 \le n, m \le k$, such that each longest path in H_n , contains at least one synchronising arc and there is at least one longest path with a same labelled synchronisation arc in H_m .

Algorithms for optimising the performance gain

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- The number of longest paths in a graph is exponential

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- Constraints for the prime factors of the synchronised product

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- · Constraints for the prime factors of the synchronised product
- Algorithm that calculates prime factors.
- An example of the decomposition of a graph







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Decomposition of a component into its prime factors



Memory usage versus performance using decomposition



Thank you for listening!

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