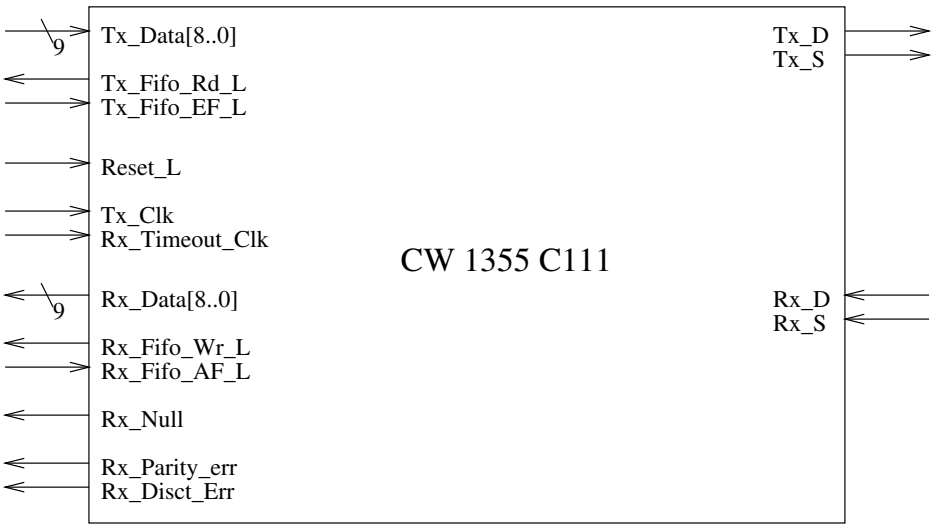
CW 1355 C111
DS-link Interface

The CW 1355 C111 is a stand-alone integrated circuit providing an interface to a (IEEE 1355) DS-link. Implemented in a small (44-pin, PLCC) programmable logic device this provides a simple, low-cost interface for dedicated systems.

All low-level flow control and error detection is handled within the device, the user supplies and receives a stream of data and packet-marker tokens. The interface is configured for direct connection to send and receive FIFO's.



Pin Descriptions

Rx_D, Rx_S — Received data and strobe signals.

Tx_D, Tx_S — Transmitted data and strobe signals.

Rx_Data[8:0] — Incoming data appears as a 9-bit word, the ninth bit (*Rx_Data[8]*) indicates how to interpret the remaining eight bits.

Tx_Data[8:0] — Outgoing data is presented as a 9-bit word, the ninth bit (*Tx_Data[8]*) indicates how to interpret the remaining eight bits.

Rx_Data and Tx_Data									Interpretation
[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Data is contained in bits 7 to 0
1	x	x	x	x	x	x	x	0	EOP
1	x	x	x	x	x	x	x	1	EOM

Rx_Fifo_Wr_L — Data is written to the receive FIFO under the control of this active-low output signal. This is low for 2-bit periods of the received data.

Rx_Fifo_AF_L — This input indicates that the receive FIFO is almost full, it must go low when there are less than 16 words available.

Tx_Fifo_Rd_L — Data is read from the transmit FIFO under the control of this active-low output signal. This is low for 2-bit periods of transmit clock (*Tx_Clk*).

Tx_Fifo_EF_L — A low-level on this pin indicates that the FIFO is empty. In other words, a high level indicates that the FIFO contains data to be sent.

Tx_Clk — This sets the transmission speed, the transmit bit rate is equal to the frequency supplied at this pin.

Rx_Timeout_Clk — Line disconnection is detected by monitoring incoming signals for activity. If no activity is seen in the period between successive rising edges of the *Rx_Timeout_Clk* a disconnect error is reported. IEEE 1355 gives a period of 800ns, requiring a 1.25MHz clock at this pin.

Rx_Null — After reset is de-asserted the receiver searches for a valid incoming Null character. A running pattern match is performed so it is unimportant exactly when the receiver starts - it will synchronise with a transmitter. After a Null has been seen the *Rx_Null* output will go high and stay at that value (regardless of whether errors are seen) until reset is asserted. No data can be received, nor any notice taken of parity or disconnect errors until a valid Null has been received.

Rx_Parity_Err — If, after a valid input has been seen, a parity error is detected in the data then the *Rx_Parity_Err* pin will go high and remain there until reset is asserted.

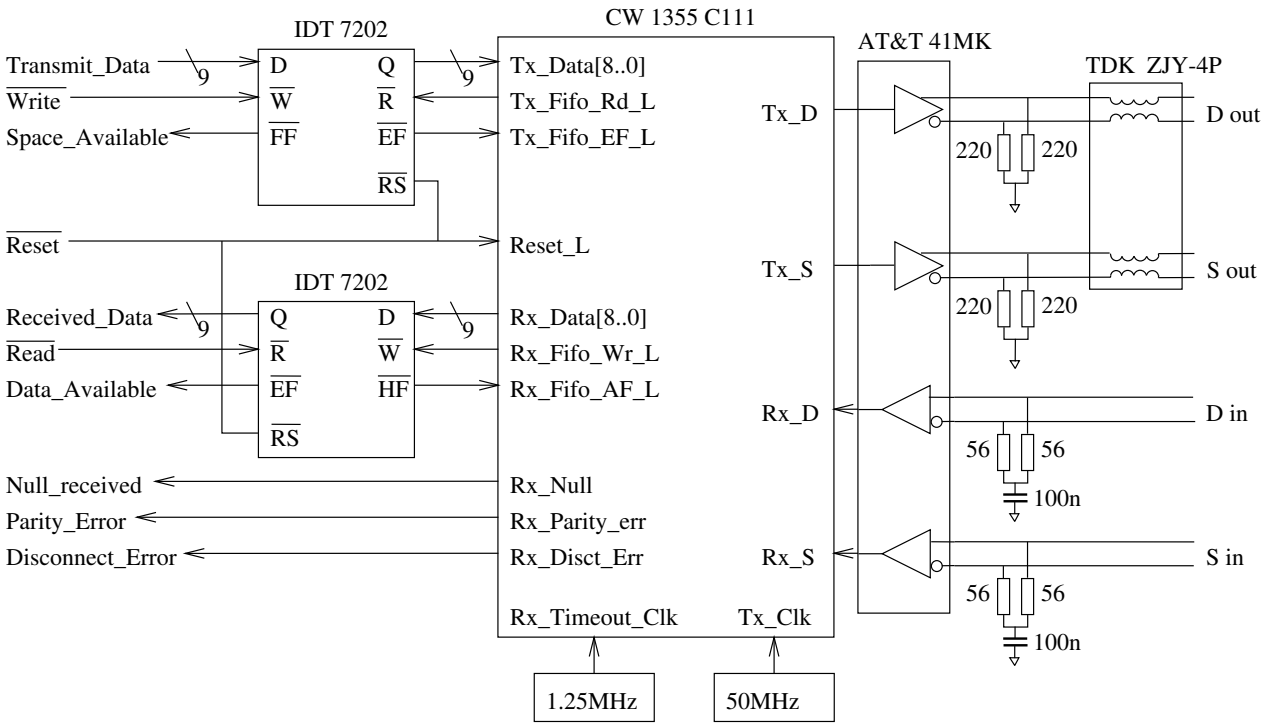
Rx_Fifo_Wr_L will not be asserted if *Rx_Parity_Err* is high.

Rx_Disct_Err — If, after a valid input has been seen, data is not received for at least the timeout period (as determined by the *Rx_Timeout_Clk*) then this line will go high and remain there until reset is asserted.

Rx_Fifo_Wr_L will not be asserted if *Rx_Disct_Err* is high.

Reset_L — All activity and internal status is reset by a low-level signal on this input, normal activity resumes after this pin goes high.

Typical Application



For Further Information

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This product is a result of collaboration between 4Links and Keele University

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